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Amendments to the Claims

1. (Original) A method of mass-producing a solid state device comprising:

supplying a solid state material substrate having a top surface; and

providing a solid state material layer no more than 40 Angstroms thick having at least one atomically smooth major surface, and positioned on the top surface of the substrate;

at least a lower surface of the solid state material layer being metallurgically bonded onto a selected portion of the top surface of the solid state material substrate, sufficiently uniformly and defect-feely to provide an acceptable device yield.

2. (Original) The method of claim 1 wherein the solid state material layer has at least two of the following features: a) having an atomically smoothed bottom surface; b) having a curved top surface; c) having an atomically smooth gate bottom surface; d) made of a solid state material purified during device processing; e) made of a single strengthened material; f) has uniformly oriented elongated and narrow grains; g) is stronger than unbonded device material; and h) less than two atomic layer thick.

3. (Original) The method as in claim 1 wherein the solid state material layer has a central bottom portion of zero width.

4. (Original) The method as in claim 1 wherein the solid state material layer has an accuracy of better than a single atom on a layer dimension selected from the group consisting of

thickness, depth, curvature, shape, size, chemical composition profiling, and lateral location.

5. (Original) The method as in claim 1 where at least a portion of the solid state material layer is surfaced strengthened, whereby this surface-strengthened portion is stronger than the unbonded solid state material layer itself.

6. (Original) The method as in claim 1 where the solid state material layer is sufficiently thin and flexible to yield under stress preventing device failure.

7. (Original) The method as in claim 1 wherein the solid state material layer is a liquid-diffusion aged or burned-in solid state material.

8. (Original) The method as in claim 1 wherein the device has a thickness of substantially less than a micron forming a flexible thin-film integrated circuit device.

9. (Original) The method as in claim 1 wherein the solid state material layer has a curved major surface with a radius of curvature of less than 1 micron.

10. (Original) The method as in claim 1 wherein a material of the solid state material layer is at least one order of magnitude purer than the solid state material prior to the uniform metallurgical bonding.

11. (Original) The method as in claim 1 wherein the solid state material layer has an accuracy in thickness of two atomic or molecular layers.

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12. (Original) The method as in claim 1 wherein the solid state materials layer comprises an ion implanted region containing a material selected from the group consisting of oxygen and nitrogen.

13. (Original) The method as in claim 1 including:

providing a solid state material substrate having a common top surface;

supplying a first and a second solid state material pockets; and

positioning a first and a second solid state material pockets adjacent to each other, but laterally separated by a gap, on the common top surface of the substrate;

the solid state material layer filling and bridging the gap between the two adjacent solid state material pockets.

14. (Original) The method as in claim 13 wherein:

at least a part of the substrate is a semiconductor of a first conductivity type; and

at least one of the semiconductor material pockets is of a second conductivity type forming at least one PN junction region where the part of the substrate contacts the at least one semiconductor material pocket.

15. (Original) The method as in claim 1 wherein the solid state material layer is selected from the group consisting of a single-material gate layer and a single-material field layer.

16. (Original) The method as in claim 1 wherein the substrate material is selected from the group consisting of Si, Ge, Si-Ge, InP, InSb, GaAs, SiC, InAs, superconductor, diamond,

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semiconductor material, intrinsic semiconductor material, substantially electrically insulating material, and substantially electrically conducting material, and mixture thereof.

17. (Original) The method as in claim 1 wherein the device is selected from the group consisting of metal-oxide-semiconductor (MOS) device, conductor-insulated-semiconductor (CIS) device, thin-film integrated circuit, flexible integrated circuit, electro optical device, single-electron device, single-hole device, single-carrier device, single-photon device, electrooptomagnetic deices and mixtures thereof.

18. (Original) The method as in claim 14 wherein:

the first and second semiconductor material pockets are respectively source and drain semiconductor pockets in a solid state device, and are separated by a gap from each other;

the solid state material layer is an electrically insulating gate layer filling and bridging the gap between the two pockets; and

the gate layer material has an atomically smooth surface on at least one of the top and major bottom surfaces thereof.

19. (Original) The method as in claim 13 wherein a major portion of each of the substrate, solid state material pockets, and solid state material layer consists essentially of a single semiconductor material doped to no more than 10 ppm of impurities thereby forming essentially a single-material device for resisting dynamic forces due to impacts, vibrations, and large and rapid accelerations and decelerations.

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20. (Original) The method as in claim 1 including forming a PN junction region having a curved adjoining surface uniformly and defect-freely bonded onto the substrate to thereby reduce but not eliminate at least one of thermal mismatch strain and volume change strain,

the remaining residual strain on the curved adjoining surface of the PN junction region improving a selected device performance.

21. (Original) The method as in claim 14 wherein the at least one PN junction region has a bottom of zero width.

22. (Original) The method as in claim 1 wherein the solid state material layer is an electrically insulating, wavy and curved field layer containing a substance selected from the group consisting of oxygen and nitrogen.

23. (Original) The method as in claim 13 wherein:

the first and second solid state material pockets are respectively source and drain semiconductor pockets in a solid state device;

the solid state material layer is a single material gate layer; and

including a conductive gate electrode of an electrically conducting material to control flow of electronic carriers from the source to the drain.

24. (Original) The method as in claim 23 wherein:

the solid state material layer is a gate layer which is atomically smooth and defect-free on at least the bottom major surface thereof;

material of the gate layer being purest at the bottom major surface facing the substrate.

25. (Original) The method as in claim 1 wherein the solid state material layer has a shallow, highly activated doped region having a significantly greater dopant concentration than the thermal equilibrium phase-diagram value.

26. (Original) The method as in claim 1 wherein the solid state material layer is a field layer separating and electrically isolating device components from each other;

the field layer on a horizontal cross-section thereof has a plurality of curved arc sections capable of changing arc lengths thereof to relieve thermal mismatch strains on the device.

27. (Original) A method for mass-producing a solid state device comprising:

supplying a solid state material substrate;

providing a solid state material pocket positioned on a selected surface of the substrate; and

forming a solid state material layer less than 40 angstroms thick and metallurgically bonded onto a selected surface of the substrate;

said metallurgical bonding being so sufficiently uniform and defect-free as to provide a thermochemically stable bonding interface and to give a manageable device yield.

28. (Original) The method as in claim27 wherein the solid state material layer is selected from the group consisting of a gate layer and a field layer.

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29. (Original) The method as in claim 27 wherein the solid state device is selected from the group consisting of atomic IC device, molecular IC device, single-electron device, single-hole device, single-carrier device, and single photon device.

30. (Original) The method as in claim 27 wherein the solid state material layer has at least one of the following features: a) has a rounded bottom with zero width; b) has at least one atomically smooth major surface; c) bonded, atom to atom, onto the substrate; d) is purified by over one order of magnitude during at least a device processing step; e) is surface strengthened; f) is liquid-diffusion formed; g) is formed using ion-implantation; h) is of an electrical insulating material; i) is free of voids and microcracks visible at 1,000 times magnification.

31. (Original) The method as in claim 27 including employing a real-time self-optimizing method to control, to an accuracy of 20 angstroms, a selected dimension of said solid state material layer;

said selected dimension being selected from the group consisting of length, width, thickness, location, shape, radius of curvature, and chemical composition profiling.

32. (Original) The method as in claim 31 including real-time sensing an optoelectrical signal from the solid state material layer.

33. Canceled

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35. Canceled

36. (Previously presented) A method for mass-producing a solid state device comprising:

supplying a solid state material substrate having a first conductivity type;

supplying a solid state material pocket of a second conductivity type and contacting a top surface of the solid substrate;

providing a signal-translating, interfacial rectifying barrier region where the solid pocket contacts the solid substrate; and

forming an electrically insulating, solid state material layer metallurgically bonded onto selected portions of both the solid substrate and the solid pocket, sufficiently uniformly and defect-freely to achieve a manageable device yield;

there being no thermally and electrically insulating voids and microcracks to cause unstable electrical contacts, unwanted instabilities; leakage current; low breakdown voltage; boron penetration; and poor device performance, reproducibility, yield, reliability, and resistance to ambient particularly as to moisture.

37. (Previously presented) The method as in claim 36 wherein the rectifying barrier region is of a type selected for the group consisting of a PN junction, a metal-oxide barrier, and a metal-semiconductor barrier, and has an accuracy of from nanometers to angstroms in a dimension or parameter selected from the group consisting of size, length, width, depth, thickness, accuracy, precision, curvature, shape, chemical

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composition profiling, and lateral location from a selected device component.

38. (Previously presented) The method as in claim 36 including using an atomic engineering technique on at least one of the solid pocket and solid state material layer for achieving at least one of the following results: replacing failure-initiating oxide or silicon surface voids and microcracks with mechanical, thermal, and electrical strengtheners; material purification; dialectical enhancement; grain refinement; preferential grain orientation to facilitate thermal and electrical conduction; subgrains of substantially uniform width, size, and height; and functional composition grading to meet special service requirements;

wherein the rectifying barrier region is bonded onto both the solid substrate and solid pocket by an atom-to-atom bonding process to enhance mechanical, electrical, and thermochemical stability thereby improving device performances as to yield, cost, and miniaturization.

39. (Previously presented) The method as in claim 36 for mass-producing an extremely small, high-precision solid state device at high yield but lost cost; and including:

atomically engineering the metallurgical bonding process between the different device materials to enhance mechanical, electrical, and thermochemical stability thereby improving device reliability on adhesion loss, texture, thermally or mechanically induced cracking, moisture adsorption, step coverage, and time-dependent behavior on thermal conductivity and breakdown voltage; and

minimizing thermal or volume expansion mismatch stresses on the device to improve device yield.

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40. (Previously presented) The method as in claim 36 including using atomic tweezers to sculpt, atom by atom or molecule by molecule, to form at least one of the solid state material substrate, pocket, and insulating layer;

forming the solid insulating layer as a gate layer having a gate length of less than 0.001 or 0.1 microns; and

controlling size of the gate layer down to less than 1 micron, with an accuracy of 1,000 angstroms down to 10 angstroms.

41. (Previously presented) The method as in claim 36 wherein the solid state material layer is an isolating groove at a specific location on the device; and has a cylindrical, elliptical, spherical, or conical shape; with a flat, spherical, rounded, or conical bottom; and

the mass-produced solid-state device is used in an industry selected from the group consisting of wireless, satellite, home appliance, building, structure, transportation vehicle, equipment, defense, and home security system.

42. (Previously presented) The method as in claim 36 including forming the solid insulating layer to have an elongated, substantially symmetrically rounded, insulating groove bottom having zero bottom width, whereby the thermal and dynamic mismatch stresses are zero in a lateral direction at the groove bottom;

the stresses being minimum and symmetrically distributed at the rounded bottom to preclude any weaker side so that the device is stronger overall.

43. (Previously presented) The method as in claim 36 including using a fusion and resolidification process to

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maximize at least one material property selected from the group consisting of material purity, mechanical strength, crystallographic perfection, self-optimized oriented grains and subgrains, and maximum thermal and electrical conductance in a preselected preferred direction. to thereby provide reliably perfect contacts and device structure, continuity, and repeatability.

44. (Previously presented) The method as in claim 36 including curving at least one of the solid pocket and the rectifying barrier region to have a radius of curvature selected from the group consisting of 10 angstroms and one micron; and

curving the solid insulating layer to have a radius of curvature selected from the group consisting of 1 cm, 0.1 cm, 0.01 cm, 0.001 cm, 1 micron, 0.1 micron, and down to one atom or molecule.

45. (Previously presented) The method as in claim 36 including: forming the solid state material pocket to occupy a major portion of a top surface area of the device chip thereby achieving hitherto impossible, device miniaturization;

only a minor portion of the top surface area being occupied by the solid state material layer and not by the solid state material pocket.

46. (Previously presented) The method as in claim 36 including: locating bottom of the solid state material layer at less than a specified distance below a designated point in the interfacial rectifying barrier region;

the specified distance being selected from the group consisting of one micron, 0.1 microns, significantly less than

0.1 microns, near zero, and between zero and 0.1 micron but closer to zero than 0.1 microns.

47. (Previously presented) The method as in claim 36 including forming a subnanometer atomic or molecular electromechanical (A/MEM) system comprising the solid state device and selected electrotechnical components including at least a structure or package, a motor, a rod, a gear, and a wheel to form the A/MEM system; and

applying the A/MEM system onto an object selected from the group consisting of human, animal, virus, bacteria, plant, equipment, and transportation vehicle;

the applying step being selected form the group consisting of implanting, inhaling, and passing along at least a part of body of the object.

48. (Previously presented) The method as in claim 47 including: telecommunicating a signal from outside of a body to the object;

directing the A/MEM system to move into a key position relative to the object; and

through another telecommunicated signal, directing the A/MEM system to perform a selected task on the object.

49. (Previously presented) The method as in claim 48 in which the selected task comprises:

real-time sensing an input data selected from the group consisting of mechanical force, pressure; heat, temperature; electrical, chemical, and electro-optical data; NMR images; brain waves; blood pressure; and skin resistance; and

performing a real-time computerized, self-optimizing R&D experiment to study a specific biochemical or biomedical action

or reaction of the object to a specific drug, virus, or biophysical and biomedical treatment for achieving an optimal mental, physical, and physiological condition selected form the group consisting of growth, learning, training, sleeping, resting, reading, enjoying, working, and restoring and maintaining health.

50. (Previously presented) The method as in claim 49 wherein the object is a transportation vehicle, and the selected task comprises achieving optimal travel condition, maximum passengers' comfort, and minimum travel time and cost, under given environments of weather, traveling route, human constraints, rules and regulations, and vehicle conditions, at least one of the following: optimal travel condition, maximum passengers' comfort, and minimum travel time and cost.

51. (Previously presented) The method as in claim 36 including selecting all materials of the solid substrate, solid pocket, and solid electrically insulating material region to have, except for ppm or ppb of impurities, the same composition, whereby all the materials have substantially the same coefficient of thermal expansion to minimize thermal mismatch stresses and also practically the same density to minimize dynamic stresses due to vibrations, impacts, and high accelerations and decelerations thereby forming an environmentally-resistant circuit device.

52. (Previously presented) The method as in claim 36 including introducing a precise amount of foreign material into the device to form a new device region in at least a part of one of the solid substrate, solid pocket, and solid state material layer, thereby achieving an exact three-dimensional

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control in shape, size, location, and chemical composition of this new region;

employing closed-loop feedback control to achieve a high accuracy of nanometers or angstroms in a dimension selected from the group consisting of size, length, width, depth or thickness, accuracy, precision, curvature, shape, chemical composition profiling, and lateral location from a selected device component; and

using the rectifying barrier region being formed or processed as a sensing medium to sense a data selected from the group consisting of optical transparency, electrical resistance, temperature, thermal conductivities, leakage currents, and other electrooptical properties of the material of at least one of the solid substrate, pocket, and layer.

53. Canceled

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57. (Previously presented) A method of mass-producing a solid state device of less than 0.1 micron in size, with nanometer accuracy, comprising:

supplying a semiconductor material substrate of one conductivity type; and

providing a semiconductor material pocket positioned on said substrate and having a conductivity type opposite to said one conductivity type thereby forming an electrically rectifying barrier between said substrate and said pocket;

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a lower surface of the semiconductor material pocket being chemically bonded, with a metallurgically graded seal, onto a selected portion of a top surface of said substrate, sufficiently uniformly and defect-freely to provide an acceptable device yield.

58. (Currently amended) A method as in claim 57, comprising: supplying said semiconductor material substrate and providing said semiconductor material pocket to have a common silicon semiconductor material;

forming an insulating material layer below said semiconductor material pocket to form a gate layer thereunder; and

choosing said insulating material layer primarily from a silicon nitride, and not a silicon dioxide, by selecting the proportion of said silicon nitride relative to the silicon dioxide from the following groups: about 100% silicon nitride; mostly of silicon nitride, and a majority of silicon nitride, to thereby improve performance of said device,

wherein said improvement is a result of the fact that during in-situ oxide formation, the silicon host material undergoes a volume expansion corresponding to a linear expansion of 29.2% when oxidizing to silicon dioxide, while similar in-situ ~~dioxide~~ nitride formation, the silicon host when oxidizing to silicon nitride gives a corresponding linear expansion of only 4.3%, or 6.79 times smaller than that during similar oxidation from silicon to silicon dioxide.

59. (Previously presented) A method as in claim 57, comprising: selecting at least one of said substrate and pocket to be of an intrinsic semiconductor material, thereby making said device more environmental friendly so that the entire

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device is more resistant to temperature, stress, impact, vibration, and high-gravity forces due to rapid acceleration and decelerations; and

minimizing device reliability issues selected from the group consisting of adhesion loss, texture, thermally or mechanically induced cracking, moisture adsorption, step coverage, and time-dependent behavior on thermal conductivity and breakdown voltage.

60. (Previously presented) A method as in claim 57, comprising: forming a closely controlled, thin insulating gate layer below said pocket to have a low defect density, to be less than 40 nm thick, and to be controlled to nanometer accuracy, wherein;

said insulating gate layer has a suitable dielectric constant and is compatible chemically with the material of at least one of said pocket to get the right interface, and layer material and structure; and

forming said device as a one-dimensional, two-dimensional, or three-dimensional, atomic or molecular diode or transistor arrays of IC selectively operable in a single-electron, single-hole, single-carrier, single-photon, or single-particle mode.

61. (Previously presented) A method as in claim 57, comprising: forming a closely controlled, thin insulating gate layer below said pocket using an ultra-shallow electrically rectifying barrier having a barrier depth of less than a value selected from the group consisting of 35 nm and 70 nm; and

atomic engineering the thin gate layer to be defect-free, suitably high dielectric constant material and uniformly put down with required stability, interface state characteristics, and channel mobility, in a thin film form with a rounded bottom

with a radius of curvature of a value selected from the group consisting of 1 micron, 0.1 microns, 0.01 microns, and 0.001 microns, in a vertical cross-section thereof, to tolerate subsequent processing and temperature cycling.